

Attorney's Docket No. 004259.P044

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Mark Peting

Application No.: 09/954,915

Filed: September 17, 2001

For: A SYSTEM AND METHOD FOR  
CONCURRENTLY DEMODULATING  
AND DECODING MULTIPLE DATA  
STREAMS

Examiner: Not Yet Assigned

Art Unit: 2661

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450 on August 11, 2004.  
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Alma Goldchain

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       A statement pursuant to 37 C.F.R. §1.97(e) or

       A check for \$180.00 for the fee under 37 C.F.R. § 1.17(p).

       37 C.F.R. §1.97(d). If so, then enclosed with this Information Disclosure Statement are the following:

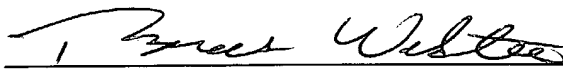
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If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

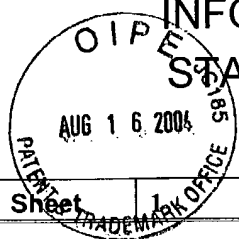
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 8/9, 2004

  
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Substitute for Form 1449/PTO



# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

**Complete if Known**

Application Number	09/954,915
Filing Date	September 17, 2001
First Named Inventor:	Mark Peting
Art Unit	2661
Examiner Name	Not Yet Assigned
Attorney Docket Number	004259.P044

of

2

**U.S. PATENT DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code <sup>2</sup> (If known)				
		US-	4,015,238	3/29/1977	Robert Curtis Davis	RECEIVED AUG 17 2004 Technology Center 2600
		US-	5,027,374	6/25/1991	Mark W. Rossman	
		US-	5,291,499 A	3/1/1994	Behrens et al.	
		US-	5,295,142	3/15/1994	Izumi Hatakeyama	
		US-	5,349,608	9/20/1994	Graham, et al.	
		US-	5,608,737 A	3/4/1997	Kimura, et al.	
		US-	5,907,586	5/25/1999	Katsuragawa, et al.	
		US-	6,189,126 B1	2/13/2001	Ulmer, et al.	
		US-	6,278,725 B1	8/21/2001	Rouphael et al.	
		US-	6,301,314 B1	10/9/2001	Murayama, Jun	
		US-	6,563,889 B1	5/13/2003	Shih, et al.	
		US-				
		US-				
		US-				
		US-				

**FOREIGN PATENT DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
		Country Code <sup>3</sup>	Number <sup>4</sup> Kind Code <sup>5</sup> (if known)				
		WO	01/59937 A2	8/16/2001	Qualcomm Inc.		

 Examiner  
Signature

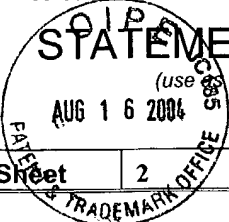
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Substitute for Form 1449/PTO <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> (use as many sheets as necessary)				<b>Complete if Known</b>	
				Application Number	09/954,915
				Filing Date	September 17, 2001
				First Named Inventor:	Mark Peting
				Art Unit	2661
				Examiner Name	Not Yet Assigned
Sheet	2	of	2	Attorney Docket Number	004259.P04
<b>NON PATENT LITERATURE DOCUMENTS</b>					
Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published			T <sup>2</sup>
		BREE, ET AL., "A Bit-Serial Architecture For A VLSI Viterbi Processor", Communications Systems Research Group, University of Saskatchewan, Saskatoon, IEEE, WESCANEX '88, 1988, pages 72-77.			
		BIVER, ET AL., "Architectural Design and Realization Of A Single-Chip Viterbi Decoder", Elsevier Science Publishers B.V., INTEGRATION, The VLSI Journal 8 (1989), October, No. 1, Amsterdam, NL, Pages 3-16.			
		BREE, ET AL., "A Modular Bit-Serial Architecture For Large Constraint-Length Viterbi Decoding", Communications Systems Research Group, University of Saskatchewan, Saskatoon, Canada, IEEE International Conference on Communications", 1990, pages 1501-1506.			
		CHOI, ET AL., "Viterbi Detector Architecture For High-Speed Optical Storage", 1997, IEEE TENCON - Speech and Image Technologies for Computing and Telecommunications, ASIC Center Corporate Technical Operations SAMSUNG Electronics, Vol. 1, Dec 1997, pages 89-92.			
		W.H. YIM and F.P. COAKLEY, "On-Board Processing For KA-Band Applications", University of Surrey, UK, Publication Date, February 11, 1993., XP 000458011, pp. 225-229.			
		HASHIDA MITSUYOSHI, "Hierarchical Network Management System and Control Method for Network Management Information," Patent Abstracts of Japan, Publication No. 07226777			

Examiner Signature	Date Considered
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